IN THEIN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 5-8 and 10 and AMEND claim 4 in accordance with the following:

1. (ORIGINAL) A semiconductor device characterized in that

connection pads for wire bonding are arranged at peripheral regions of an electrode terminal formation surface of a semiconductor chip,

test pads for testing the semiconductor chip are arranged in an inside region surrounded by said peripheral regions of said electrode terminal formation surface, and

a plurality of rewiring patterns extend from the peripheral regions to said inside region of said electrode terminal formation surface and the individual rewiring patterns connect the individual electrode terminals and the corresponding connection pads and test pads.

2. (ORIGINAL) A semiconductor device as set forth in claim 1, characterized in that the test pads are arranged in an array on said inside region.

3. (PREVIOUSLY PRESENTED) A semiconductor device as set forth in claim 1, characterized in that said electrode terminals are exposed from openings of a protective insulation layer covering said electrode terminal formation surface, said rewiring patterns extend on said protective insulation layer and are connected to said electrode terminals via said openings, said rewiring patterns and said protective insulation layer are further covered by an insulation layer, and said connection pads and said test pads connected to said rewiring patterns are exposed from openings of said insulation layer.

4. (CURRENTLY AMENDED) A semiconductor device comprised of one or a stack of a plurality of the semiconductor device as set forth in ~~any one of claims~~ claim 1 ~~to 3~~ as an element semiconductor device or a stack of one or more of each of said element semiconductor device and a semiconductor chip carried on a wiring board, said semiconductor device characterized in that

connection pads of each said element semiconductor device and connection electrodes of said wiring board are connected by wire bonding, and

each said element semiconductor device and/or each said semiconductor chip is sealed by resin on said wiring board.

5. (CANCELLED)

6. (CANCELLED)

7. (CANCELLED)

8. (CANCELLED)

9. (PREVIOUSLY PRESENTED) A semiconductor device as set forth in claim 2, characterized in that said electrode terminals are exposed from openings of a protective insulation layer covering said electrode terminal formation surface, said rewiring patterns extend on said protective insulation layer and are connected to said electrode terminals via said openings, said rewiring patterns and said protective insulation layer are further covered by an insulation layer, and said connection pads and said test pads connected to said rewiring patterns are exposed from openings of said insulation layer.

10. (CANCELLED)